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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/898,185	07/03/2001	Kouji Kumada	70904-56232	9635

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EXAMINER	
LESPERANCE, JEAN E	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/898,185	KUMADA ET AL.	
	Examiner	Art Unit	
	Jean E Lesperance	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *February 1, 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6,10-12,18-21 and 27-30* is/are rejected.

7)☒ Claim(s) *3, 5, 7-9, 13-17 and 22-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8-31-05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed February 1, 2006 is entered and claims 1-30 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 6, 11, 12, 19, 21, and 28 are rejected under 35 USC 102 (b) as being unpatentable over US Patent #5,579,027 ("Sakurai et al.").

Regarding claim 1, Sakurai et al. teach a drive circuit for use in a liquid crystal display (a method of driving an image display apparatus, and more particularly to a method of driving an image display apparatus especially suitable for an active matrix liquid display apparatus for example (column 1, lines 11-20)),

said drive circuit supplying source signal from a source driver to pixel electrodes through switching by means of thin film transistors according to scan signals from a gate driver (reference numeral 110 represents a sample holding circuit, the first stage of

which is composed of a sampling transistor 115, a capacitor 116 and a buffer amplifier 117. An output terminal of the sample holding circuit 110 is connected to a signal line 20 shown in FIG. 13 (column 7, lines 11-20)),

said drive circuit comprising adjusting means (amplifier Fig.13 (117)) for adjusting potential differences between the pixel electrodes and a common electrode, a voltage level altering means (amplifier Fig.13 (117)) for shifting voltage levels of the source signals supplied by the source driver equally for all the pixel electrodes, where the buffer amplifier would amplify or adjust or change the voltage level of all the column lines in the signal line 20 (see Fig.13)).

Regarding claim 6, Sakurai et al. teach the voltage divider means is capable of producing a plurality of mutually different sets voltages as the source drive reference voltages one of the sets as outputs (a T flip-flop which receives pulses VD (the width of which is determined arbitrarily) at a period of one field, so that an output signal 32 is inverted at each field (column 5, lines 41-45)).

Regarding claims 11,19, and 28, Sakurai et al. teach the common electrode signal generator means is built in the source driver (the sample holding circuit (source driver) Fig.4 (10) .

Regarding claim 12, Bitzakidis et al. teach a liquid crystal display, for use in a liquid crystal comprising a drive circuit display (a method of driving an image display apparatus, and more particularly to a method of driving an image display apparatus especially suitable for an active matrix liquid display apparatus for example (column 1, lines 11-20)),

said drive circuit supplying source signals from a source driver to pixel electrodes through switching by means of thin film transistors according to scan signals from a gate driver (reference numeral 110 represents a sample holding circuit, the first stage of which is composed of a sampling transistor 115, a capacitor 116 and a buffer amplifier 117. An output terminal of the sample holding circuit 110 is connected to a signal line 20 shown in FIG. 13 (column 7, lines 11-20)),

said drive circuit comprising adjusting means (amplifier Fig.13 (117)) for adjusting potential differences between the pixel electrodes and a common electrode, a voltage level altering means (amplifier Fig.13 (117)) for shifting voltage levels of the source signals supplied by the source driver equally for all the pixel electrodes, where the buffer amplifier would amplify or adjust or change the voltage level of all the column lines in the signal line 20 (see Fig.13)).

Regarding claim 21, Bitzakidis et al. teach electronics, comprising a liquid crystal display including a drive circuit for use display (a method of driving an image display apparatus, and more particularly to a method of driving an image display apparatus especially suitable for an active matrix liquid display apparatus for example (column 1, lines 11-20)),

said drive circuit supplying source signals from a source driver to pixel electrodes through switching by means of thin film transistors according to scan signals from a gate driver (reference numeral 110 represents a sample holding circuit, the first stage of which is composed of a sampling transistor 115, a capacitor 116 and a buffer amplifier

117. An output terminal of the sample holding circuit 110 is connected to a signal line 20 shown in FIG. 13 (column 7, lines 11-20)),

said drive circuit comprising adjusting means (amplifier Fig.13 (117)) for adjusting potential differences between the pixel electrodes and a common electrode, a voltage level altering means (amplifier Fig.13 (117)) for shifting voltage levels of the source signals supplied by the source driver equally for all the pixel electrodes, where the buffer amplifier would amplify or adjust or change the voltage level of all the column lines in the signal line 20 (see Fig.13)).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 4, 10, 18, 20, 27, 29, and 30 rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent # 5,579,027 ("Sakurai et al.") in view of US Patent # 5,798,740 ("Bitzakidis et al.").

Regarding claim 2, Sakurai et al. fails to teach the adjusting means adjusts potential differences between the pixel electrodes and the common electrode to compensate for effects of variations in drain voltages caused by film transistors. However, Bitzakidis et al. teach the adjusting means adjusts the potential differences between the pixel electrodes and the common electrode to compensate for effects of

variations in drain voltages caused by film transistors (data signal adjustment circuit Fig.1 (40) to the capacitive capacitor Fig.2 (Cs) across the transistor (25).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize the data signal adjusting circuit as taught by Bitzakidis et al. in the sample sampling circuit disclosed by Sakurai et al. because this would provide a method of driving an image display apparatus capable of sampling image signals, which correspond to the lines, while deviating the sampling time in a manner which corresponds to the deviation of the pixels in the horizontal direction, and which is therefore capable of improving the resolution in the horizontal direction (column 2, lines 31-38).

Regarding claim 4, Bitzakidis et al. teach the adjusting means adjusts the potential differences between the pixel electrodes and the common electrode to compensate for irregularities in DC voltage caused asymmetry in properties between an active matrix substrate and an opposite substrate sandwiching a liquid crystal layer(data signal adjustment circuit Fig.1 (40) to the capacitive capacitor Fig.2 (Cs) across the transistor (25).

Regarding claim 10, Bitzakidis et al. teach common electrode signal generator means including switching means only for switching between the ground potential and the positive power source to provide fixed potential to the common electrode (data signal adjustment circuit Fig.1 (40) to the capacitive capacitor Fig.2 (Cs) across the transistor (25).

Regarding claim 18, Bitzakidis et al. teach said drive circuit further including common electrode signal generator means including switching means only for switching between the ground potential and the positive power source to provide a fixed potential to the common electrode (the panel 10 is of a known kind and can be of the type using TFTs or two terminal non-linear devices as switching devices for the picture elements. FIGS. 2A and 2B show respectively the circuit configurations of a typical picture element of a TFT active matrix panel and a two terminal non-linear device active matrix panel. In the former, FIG. 2A, the gate of the TFT, 25, is connected to a row address conductor 14 and its source and drain terminals are connected respectively to a column address conductor 16 and an electrode of a display element 30 (column 6, lines 27-42)).

Regarding claim 20, Bitzakidis et al. teach the liquid crystal display is one of reflective, opaque, reflective/transparent, or transparent types (a display picture the vertical crosstalk manifests itself most obviously as bands of different luminance extending above and below particularly bright or dark areas of the picture (column 2, lines 29-32)).

Regarding claim 27, Bitzakidis et al. teach said drive circuit further including common electrode signal generator means including switching means only for switching between the ground potential and the positive power source to provide a fixed potential to the common electrode (the panel 10 is of a known kind and can be of the type using TFTs or two terminal non-linear devices as switching devices for the picture elements. FIGS. 2A and 2B show respectively the circuit configurations of a typical picture element of a TFT active matrix panel and a two terminal non-linear device active matrix panel. In

the former, FIG. 2A, the gate of the TFT, 25, is connected to a row address conductor 14 and its source and drain terminals are connected respectively to a column address conductor 16 and an electrode of a display element 30 (column 6, lines 27-42)).

Regarding claim 29, Bitzakidis et al. teach the liquid crystal display is one of reflective, opaque, reflective/transparent, or transparent types (a display picture the vertical crosstalk manifests itself most obviously as bands of different luminance extending above and below particularly bright or dark areas of the picture (column 2, lines 29-32)).

Regarding claim 30, Bitzakidis et al. teach the electronics include a mobile wherein telephone, a personal data assistant, a notebook personal computer, a portable television set, and a portable game machine (a television (column 1, line 56).

Allowable Subject Matter

4. Claims 3, 5, 7-9, 13-17 and 22-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (571) 272-7692. The examiner can normally be reached on from Monday to Friday between 10:OOAM and 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (571) 272-7691.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 273-8300 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance

Date 3/30/2006

Art Unit 2629

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600